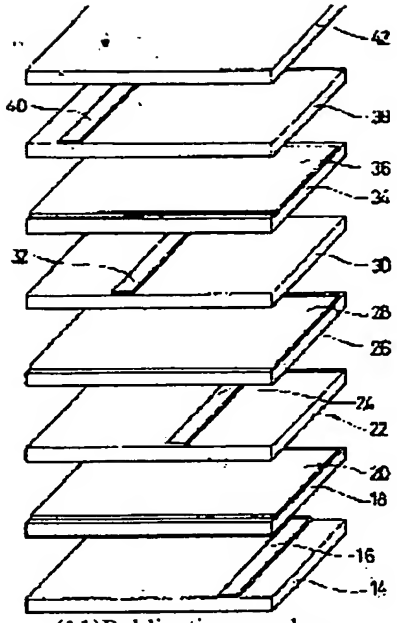

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(54) MULTILAYER THREE-TERMINAL CAPACITOR ARRAY

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a multilayer three-terminal capacitor array having a small size and a small stroke.
SOLUTION: A multilayer three-terminal capacitor array includes a multilayer body 12. The multilayer body 12 is formed by stacking a plurality of dielectric layers 14, 18, 22, 26, 30, 34, 38, and 42. Signal electrodes 16, 24, 32, and 40 are formed on the dielectric layers 14, 22, 30, and 38, respectively, with one signal electrode on each dielectric layer. Ground electrodes 20, 28, and 36 are formed on the dielectric layers 18, 26, and 34, respectively, arranged between the signal electrodes 16, 24, 32, and 40. On the outer side of the multilayer body, an outer electrode connected to both ends of each of the signal electrodes 16, 24, 32, and 40, and an outer electrode connected to the ground electrodes 20, 28, and 36 are formed. The number of ground electrodes between the signal electrodes can be two or more.

CLAIMS

[Claim(s)]
[Claim 1] It has the laminating field containing two or more signal electrodes formed on two or more dielectric layers and the above-mentioned dielectric layer, and the grand electrode formed all over the above-mentioned dielectric layer in which the above-mentioned signal electrode is not formed. In the above-mentioned dielectric layer in which the above-mentioned signal electrode was formed, only the one above-mentioned signal electrode is formed on the one above-mentioned dielectric layer. And the laminating 3 terminal capacitor array in which the laminating of the above-mentioned dielectric layer was carried out, the laminating field was formed in so that the above-mentioned grand electrode might be arranged among two or more above-mentioned signal electrodes, and the external electrode connected to the superficies of the above-mentioned laminating

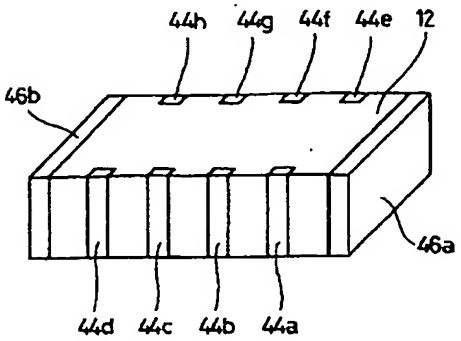
field at each of the above-mentioned signal electrode and the above-mentioned grand electrode was formed.
[Claim 2] The laminating 3 terminal capacitor array according to claim 1 by which two or more above-mentioned grand electrodes are arranged between the above-mentioned signal electrodes.
[Claim 3] The laminating 3 terminal capacitor array according to claim 1 or 2 by which two or more above-mentioned signal electrodes were connected to the same above-mentioned external electrode.

DESCRIPTION OF DRAWINGS

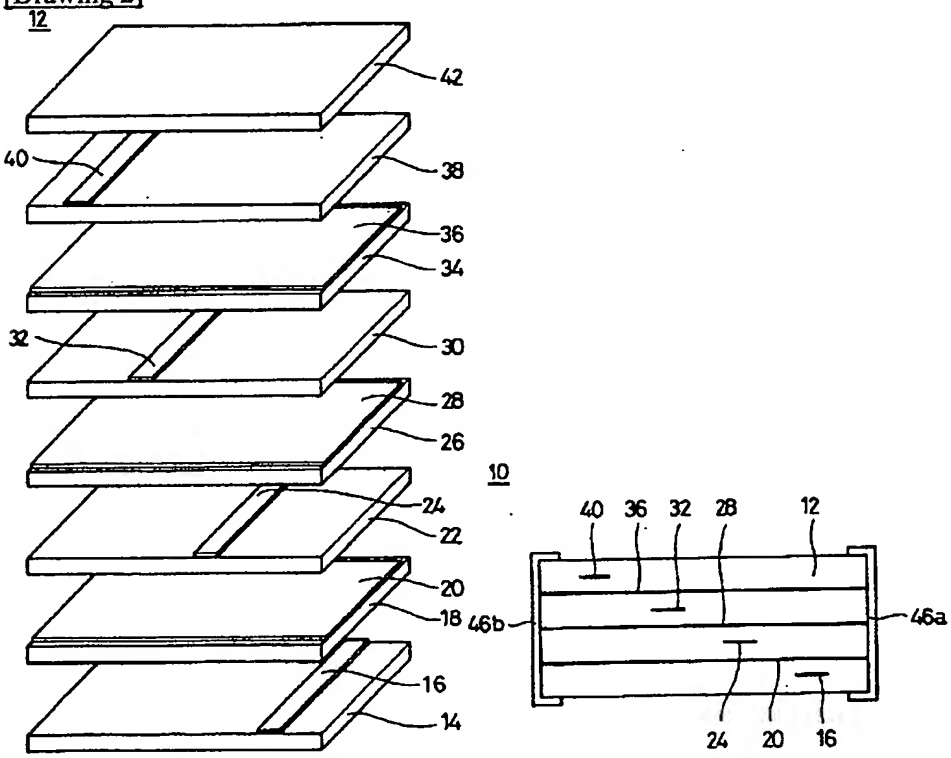
[Brief Description of the Drawings]
[Drawing 1] It is the perspective diagram showing an example of the laminating 3 terminal capacitor array of this invention.
[Drawing 2] It is the decomposition perspective diagram showing the laminating field of a laminating 3 terminal capacitor array shown in drawing 1 .
[Drawing 3] It is the sectional-drawing solution view of a laminating 3 terminal capacitor array showing in drawing 1 .
[Drawing 4] It is the equal circuit view of a laminating 3 terminal capacitor array showing in drawing 1 .
[Drawing 5] It is the sectional-drawing solution view showing other examples of the laminating 3 terminal capacitor array of this invention.
[Drawing 6] It is the equal circuit view showing the relation between two 3 terminal capacitors formed in the laminating 3 terminal capacitor array shown in drawing 5 .
[Drawing 7] It is the equal circuit view showing the relation between two 3 terminal capacitors formed in the laminating 3 terminal capacitor array shown in drawing 3 .
[Drawing 8] It is the sectional-drawing solution view showing the modification of a laminating 3 terminal capacitor array shown in drawing 5 .
[Drawing 9] It is the perspective diagram showing an example of the conventional laminating 3 terminal capacitor array.
[Drawing 10] It is the decomposition perspective diagram of the laminating field used for the conventional laminating 3 terminal capacitor array shown in drawing 9 .
[Drawing 11] It is the sectional-drawing solution view of the conventional laminating 3 terminal capacitor array showing in drawing 9 .
[Drawing 12] It is the sectional-drawing solution view showing the laminating 3 terminal capacitor array which has improved the cross talk of a laminating 3 terminal capacitor array shown in drawing 11 .
[Description of Notations]
10 Laminating 3 Terminal Capacitor Array
12 Laminating Field
14 1st Dielectric Layer
16 1st Signal Electrode
18 2nd Dielectric Layer
20 Grand Electrode
22 3rd Dielectric Layer
24 2nd Signal Electrode
26 4th Dielectric Layer
28 Grand Electrode
30 5th Dielectric Layer
32 3rd Signal Electrode
34 6th Dielectric Layer
36 Grand Electrode
38 7th Dielectric Layer
40 4th Signal Electrode
42 Dielectric Layer of Octavus
44a-44h External electrode
46a, 46b External electrode

48, 50, 52, 54 Signal electrode
56a, 56b, 58a, 58b Grand electrode
60a, 60b, 62a, 62b Grand electrodeDRAWINGS

[Drawing 1]



[Drawing 2]



[Drawing 3]

[Drawing 4]
DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] This invention relates to the laminating 3 terminal capacitor

array in which two or more 3 terminal capacitors used as a noise filter etc. were formed in 1 chip, especially about à laminating 3 terminal capacitor array, for example.
[0002]
[Description of the Prior Art] Drawing 9 is a perspective diagram showing an example of the conventional laminating 3 terminal capacitor array. The laminating 3 terminal capacitor array 1 includes the laminating field 2. The laminating field 2 contains two or more dielectric layers 3a-3d, as shown in drawing 10 . On 1st dielectric layer 3a, the signal electrodes 4a-4d of the shape of four straight line are formed. Moreover, on 2nd dielectric layer 3b, the grand electrode 5 is mostly formed on the whole surface except for the both sides which signal electrodes 4a-4d exposed. Furthermore, on 3rd dielectric layer 3c, another signal electrodes 6a-6d are formed in the position corresponding to signal electrodes 4a-4d. And 3d of the 4th dielectric layer is laid in a signal electrodes [these / 6a-6d] top. The laminating of these dielectric layers 3a-3d is carried out, and the laminating field 2 is formed.
[0003] The external electrodes 7a-7h to which the signal electrodes 4a-4d and the signal electrodes 6a-6d are connected are formed in the superficies of the laminating field 2. Furthermore, two external electrodes 8 to which the grand electrode 5 is connected are formed in the superficies of the laminating field 2. Signal electrodes 4a and 6a are connected to the external electrodes 7a and 7e. Therefore, it flows between external electrode 7a and 7e, and electrostatic capacity is formed between the external electrodes 7a and 7e and the external electrode 8. Similarly, signal electrodes 4b and 6b are connected to the external electrodes 7b and 7f, signal electrodes 4c and 6c are connected to the external electrodes 7c and 7g, and signal electrodes 4d and 6d are connected to the external electrodes 7d and 7h.
[0004] This laminating 3 terminal capacitor array 1 is used as a noise filter. That is, the external electrode 8 is connected to a ground potential, and the noise contained in a signal is removed by passing a signal between external electrode 7a and 7e by the electrostatic capacity formed between the external electrodes 7a and 7e and the external electrode 8. In the laminating 3 terminal capacitor array 1, since two or more such 3 terminal capacitors are formed, the noise of two or more signals in one chip is removable.
[0005] As this laminating 3 terminal capacitor array 1 is shown in drawing 11 , signal electrodes 4a-4d are formed in the same side, and signal electrodes 6a-6d are formed in same another field. Therefore, stray capacity occurs between signal electrodes [4a-4d] adjoining things. the same -- signal electrodes 6a-6d -- although it adjoins, stray capacity occurs in between If a signal is passed to two or more 3 terminal capacitors for this stray capacity, the signal which flows to 3 terminal capacitor will travel to another 3 terminal capacitor, and the so-called cross talk will occur. In order to make small stray capacity between such signal electrodes, as shown in drawing 12 , there are some which formed signal electrodes 4a and 4c and the signal electrodes 4b and 4d on the different field, and formed signal electrodes 6a and 6c and the signal electrodes 6b and 6d on the different field. And the grand electrode 5 is formed between the fields in which each signal electrode was formed, respectively.
[0006] In this laminating 3 terminal capacitor array 1, since the grand electrode 5 is formed, for example between two signal electrodes 4a and 4b, stray capacity does not occur between such signal-electrode 4a and 4b. Moreover, since the distance between signal-electrode 4a which adjoins in the same side, and 4c becomes large, such 4a between signal electrodes and the stray capacity generated among 4c become small. The stray capacity which is the same about other signal electrodes and stray capacity does not generate between the signal electrodes in the both sides of a grand electrode, but is generated since the distance between the signal electrodes which adjoin in the same side is large is the parvus. Therefore, in the laminating 3 terminal capacitor array 1 shown in drawing 12 , a cross talk can be made small compared with what is shown in drawing 11 .
[0007]
[Problem(s) to be Solved by the Invention] However, the miniaturization is advanced also for the laminating 3 terminal capacitor array by the request of a miniaturization of electronic parts. In this case, the distance between the signal electrodes in the same side becomes small, stray capacity becomes large, and a cross talk becomes large. Furthermore, the signal electrode in the both sides of a grand electrode will form electrostatic capacity between the same grand electrodes. Therefore, a signal may be transmitted between the signal electrodes in the both sides through a grand electrode, and a cross talk may occur too.
[0008] So, the main purpose of this invention is small and is offering the parvus laminating 3 terminal capacitor array of a cross talk.
[0009]

[Means for Solving the Problem] Two or more signal electrodes by which this invention is formed on two or more dielectric layers and a dielectric layer, It has the laminating field containing the grand electrode formed all over the dielectric layer in which a signal electrode is not formed. In the dielectric layer in which the signal electrode was formed, only one signal electrode is formed on one dielectric layer. And it is the laminating 3 terminal capacitor array in which the laminating of the dielectric layer was carried out, the laminating field was formed in so that a grand electrode might be arranged among two or more signal electrodes, and the external electrode connected to the superficies of the laminating field at each of a signal electrode and a grand electrode was formed. In this laminating 3 terminal capacitor array, two or more grand electrodes may be made to be arranged between signal electrodes. Furthermore, you may connect two or more signal electrodes to the same external electrode.

[0010] Since only one signal electrode is formed on one dielectric layer and the grand electrode is arranged among two or more signal electrodes, stray capacity does not occur among two or more signal electrodes. Therefore, the cross talk by the stray capacity between signal electrodes can be reduced. And since only one signal electrode is formed in one dielectric layer, even if it miniaturizes, occurrence of the stray capacity between signal electrodes can be prevented. In such a laminating 3 terminal capacitor array, if two or more grand electrodes are formed between signal electrodes, each signal electrode can form electrostatic capacity between different grand electrodes, and can reduce the cross talk through the grand electrode. Furthermore, while capacity can be enlarged by connecting two or more signal electrodes to the same external electrode, the cross section of the signal electrode of one 3 terminal capacitor becomes large, and can enlarge current capacity.

[0011] The above-mentioned purpose of this invention, the other purposes, the characteristic feature, and an advantage will become much more clear from the detailed explanation of the following examples performed with reference to a drawing.

[0012]

[Embodiments of the Invention] Drawing 1 is a perspective diagram showing an example of the laminating 3 terminal capacitor array of this invention. The laminating 3 terminal capacitor array 10 includes the laminating field 12. The laminating field 12 contains the 1st dielectric layer 14, as shown in drawing 2 . On the 1st dielectric layer 14, the 1st signal electrode 16 of the shape of a straight line prolonged in the width-of-face orientation is formed. In the fraction near the end side of the 1st dielectric layer 14, the 1st signal electrode 16 is formed so that it may become almost parallel to the end. And the 1st signal electrode 16 is formed so that it may expose to the both sides of the width-of-face orientation of the 1st dielectric layer 14.

[0013] On the 1st dielectric layer 14 in which the 1st signal electrode 16 was formed, the laminating of the 2nd dielectric layer 18 is carried out. On the 2nd dielectric layer 18, the grand electrode 20 is mostly formed except for the both sides which the 1st signal electrode 16 exposed on the whole surface. Furthermore, on the grand electrode 20, the laminating of the 3rd dielectric layer 22 is carried out. On the 3rd dielectric layer 22, the 2nd signal electrode 24 is formed in parallel with the 1st signal electrode 16. This 2nd signal electrode 24 is formed so that it may expose to the both sides of the width-of-face orientation of the 3rd dielectric layer 22. And the 2nd signal electrode 24 is formed in the position which shifted from the 1st signal electrode 16.

[0014] On the 3rd dielectric layer 22 in which the 2nd signal electrode 24 was formed, the laminating of the 4th dielectric layer 26 is carried out. On the 4th dielectric layer 26, the grand electrode 28 is mostly formed on the whole surface except for the both sides which the 1st and 2nd signal electrodes 16 and 24 exposed. Furthermore, on the grand electrode 28, the laminating of the 5th dielectric layer 30 is carried out. On the 5th dielectric layer 30, the 3rd signal electrode 32 is formed in parallel with the 1st and 2nd signal electrodes 16 and 24. This 3rd signal electrode 32 is formed so that it may expose to the both sides of the width-of-face orientation of the 5th dielectric layer 30. And the 3rd signal electrode 32 is formed in the position which shifted from the 1st and 2nd signal electrodes 16 and 24.

[0015] On the 5th dielectric layer 30 in which the 3rd signal electrode 32 was formed, the laminating of the 6th dielectric layer 34 is carried out. On the 6th dielectric layer 34, the grand electrode 36 is mostly formed on the whole surface except for the both sides which the 1st, the 2nd, and 3rd signal electrodes 16, 24, and 32 exposed. Furthermore, on the grand electrode 36, the laminating of the 7th dielectric layer 38 is carried out. On the 7th dielectric layer 38, the 4th signal electrode 40 is formed in parallel with the 1st, the 2nd, and 3rd signal electrodes 16, 24, and 32. This 4th signal electrode 40 is formed so that it may expose to the both sides of the width-of-face orientation of the 7th dielectric layer 38. And the 4th signal electrode 40 is formed in the position

which shifted from the 1st, the 2nd, and 3rd signal electrodes 16, 24, and 32. On the 7th dielectric layer 38 in which this 4th signal electrode 40 was formed, the laminating of the dielectric layer 42 of the octavus is carried out.

[0016] The external electrodes 44a, 44b, 44c, and 44d and the external electrodes 44e, 44f, 44g, and 44h are formed in the two side faces in which the signal electrodes 16, 24, 32, and 40 of the laminating field 42 were pulled out. The end of the 1st signal electrode 16 is connected to external electrode 44a, and the other end of the 1st signal electrode 16 is connected to external electrode 44e. Moreover, the end of the 2nd signal electrode 24 is connected to external electrode 44b, and the other end of the 2nd signal electrode 24 is connected to 44f of external electrodes. The end of the 3rd signal electrode 32 is connected to external electrode 44c, and the other end of the 3rd signal electrode 32 is connected to 44g of external electrodes. Moreover, the end of the 4th signal electrode 40 is connected to 44d of external electrodes, and the other end of the 4th signal electrode 40 is connected to 44h of external electrodes.

[0017] Furthermore, another external electrodes 46a and 46b are formed in the two side faces in which the external electrodes 44a-44h of the laminating field 12 are not formed. Three grand electrodes 20, 28, and 36 are connected to these external electrodes 46a and 46b. As the interior of this laminating 3 terminal capacitor array 10 is shown in drawing 3 , the 1st signal electrode 16, the 2nd signal electrode 24, the 3rd signal electrode 32, and the 4th signal electrode 40 are arranged in the shape of a step, and the grand electrodes 20, 28, and 36 are arranged among each signal electrodes 16, 24, 32, and 40.

[0018] In this laminating 3 terminal capacitor array 10, the external electrodes 46a and 46b are connected to a ground potential. And a signal is passed for external electrode 44b and 44f between external electrode 44a and 44e in external electrode 44c and 44g and in 44d of external electrodes, and 44h. Therefore, as shown in drawing 4 , a signal is passed by signal electrodes 16, 24, 32, and 40, and electrostatic capacity is formed between these signal electrodes 16, 24, 32, and 40 and the grand electrodes 20, 28, and 36. Therefore, if a signal is inputted into the external electrodes 44a, 44b, 44c, and 44d, the noise contained in it will be removed by electrostatic capacity, and the signal without a noise will be outputted from the external electrodes 44e, 44f, 44g, and 44h.

[0019] In this laminating 3 terminal capacitor array 10, only one signal electrode is formed on one dielectric layer, and the grand electrode is arranged between each signal electrode. That is, since a grand electrode surely exists between adjoining signal electrodes, stray capacity does not occur between signal electrodes. Therefore, even if it miniaturizes the laminating 3 terminal capacitor array 10, by the stray capacity between signal electrodes, it can prevent transmitting a signal from one signal electrode to other signal electrodes, and the so-called cross talk can be decreased.

[0020] However, the 1st signal electrode 16 and 2nd signal electrode 24 share the grand electrode 20 between the laminating 3 terminal capacitor array 10 shown in the drawing 2 and the drawing 3 , the 2nd signal electrode 24 and 3rd signal electrode 32 share the grand electrode 28 between it, and the 3rd signal electrode 32 and 4th signal electrode 40 are sharing the grand electrode 36 between it. Therefore, the cross talk through these grand electrodes 20, 28, and 36 may be unable to be prevented. Then, as shown in drawing 5 , it can consider forming two or more grand electrodes between each signal electrode.

[0021] In this laminating 3 terminal capacitor array 10, two grand electrodes 20a and 20b are formed between the 1st signal electrode 16 and the 2nd signal electrode 24. Similarly, between the 2nd signal electrode 24 and the 3rd signal electrode 32, two grand electrodes 28a and 28b are formed, and two grand electrodes 36a and 36b are formed between the 3rd signal electrode 32 and the 4th signal electrode 40. And these grand electrodes 20a, 20b, 28a, 28b, 36a, and 36b are connected to the external electrodes 46a and 46b, and the external electrodes 46a and 46b are connected to a ground potential.

[0022] Also in this laminating 3 terminal capacitor array 10, since the grand electrode is formed between each signal electrode, stray capacity cannot occur between signal electrodes, but the cross talk between signal electrodes can be decreased. Furthermore, two grand electrodes are formed between each signal electrode, and moreover, since these grand electrodes are these potentials, they can decrease the cross talk between grand electrodes.

[0023] In order to explain this, the equal circuit at the time of forming two grand electrodes between signal electrodes is shown in drawing 6 , and the equal circuit at the time of forming one grand electrode between signal electrodes is shown in drawing 7 . In these equal circuits, C1 is electrostatic capacity formed between one

signal electrode and a grand electrode, and C2 is electrostatic capacity formed between another signal electrode and a grand electrode. Moreover, L1 and L2 are the residual inductances of a grand electrode. L1 is an inductance which exists between the external electrodes 46a or 46b and the signal electrode near it here, and L2 is the inductance of the grand electrode which exists in the domain of the spacing of two signal electrodes. Furthermore, L0 is the residual inductance of the electrode of the circuit board which mounts the laminating 3 terminal capacitor array 10.

[0024] In drawing 7 , since the number of the grand electrodes between signal electrodes is one, two electrostatic capacity C1 and C2 is connected with one inductance L2. To it, since the number of the grand electrodes between signal electrodes is two, two electrostatic capacity C1 and C2 is connected in drawing 6 with the inductance L1 which exists in two grand electrodes, and the inductance L2 which exists in one grand electrode.

[0025] In the equal circuit shown in drawing 7 , the noise transmitted from electrostatic capacity C2 to the grand electrode flows to a gland through inductances L2, L1, and L0, and is not transmitted from electrostatic capacity C1 to other signal electrodes. However, if the impedance of electrostatic capacity C1 will become small if the frequency of a noise becomes high, and it becomes the impedance of inductance L1+L0 closely, as the arrow head shows, a noise will become easy to travel to other signal electrodes through electrostatic capacity C1. As long as the inductance L1 between electrostatic capacity C1 and the inductance L0 of the circuit board is larger than L0 even if the impedance of electrostatic capacity C1 benefits a RF noise small since electrostatic capacity C1 and C2 is not connected only with an inductance L2 in the equal circuit shown in drawing 6 to it, as the arrow head shows, a noise does not travel to an electrostatic-capacity C1 side.

[0026] Thus, the cross talk through the cross talk and grand electrode between signal electrodes can be decreased by forming only one signal electrode in one dielectric layer, and forming two grand electrodes between signal electrodes. In addition, the number of the grand electrodes between signal electrodes cannot be overemphasized by that not only two but three grand electrodes or more may be formed.

[0027] Moreover, in order to increase the current capacity of a signal electrode, as shown in drawing 8 , you may form two or more signal electrodes between the external electrodes for I/O. Here, in addition to the laminated structure of the laminating 3 terminal capacitor array shown in drawing 5 , the laminating of many dielectric layers is carried out further, and signal electrodes 48, 50, 52, and 54 are formed. Furthermore, in addition to the grand electrodes 22a, 22b, 28a, 28b, 36a, and 36b, the grand electrodes 56a, 56b, 58a, 58b, 60a, 60b, 62a, and 62b are formed. Every two of these grand electrodes are formed between each signal electrode, respectively.

[0028] Signal electrodes 16 and 48 are formed in the position which corresponds mutually, and are connected to the external electrodes 44a and 44e. Similarly, signal electrodes 24 and 50, the signal electrodes 32 and 52, and the signal electrodes 40 and 54 are formed in the position which corresponds mutually, and are connected to the external electrodes 44b and 44f, the external electrodes 44c and 44g, and the external electrodes 44d and 44h, respectively. In this laminating 3 terminal capacitor array 10, since two signal electrodes 16 and 48 are connected, for example between external electrode 44a and 44e, compared with the laminating 3 terminal capacitor array shown in the drawing 5 to which only one signal electrode 16 was connected, the cross section of a signal electrode becomes twice by high capacity. Therefore, the current capacity of the signal electrode between external electrode 44a and 44e becomes large, and the signal of a high current can be passed.

[0029] Of course, the number of the signal electrodes connected between external electrodes may be three or more, and should just adjust the number of the signal electrodes connected between external electrodes according to desired current capacity. In order to increase the number of the signal electrodes between external electrodes, a cross talk can be prevented as mentioned above by forming a grand electrode between each signal electrode that what is necessary is just to increase the number of laminatings of the dielectric layer in which the signal electrode was formed. In addition, the current capacity can be enlarged by increasing the number of the signal electrodes connected between external electrodes also about the laminating 3 terminal capacitor array in which one grand electrode was formed between signal electrodes.

[0030]

[Effect of the Invention] According to this invention, by forming only one signal electrode on one dielectric layer, and moreover forming a grand electrode between signal electrodes, stray capacity does not occur between signal electrodes, but the cross talk between signal electrodes can be stopped. Therefore, distance between

signal electrodes can be made small and a miniaturization of a laminating 3 terminal capacitor array can be attained. Furthermore, by setting or more to two the grand electrode formed between signal electrodes, the adjoining grand electrode serves as this potential, and the cross talk through the grand electrode can be stopped. Moreover, by connecting two or more signal electrodes between the external electrodes which constitute one 3 terminal capacitor, current capacity can be enlarged and the signal of a high current can be passed.

[Translation done.]

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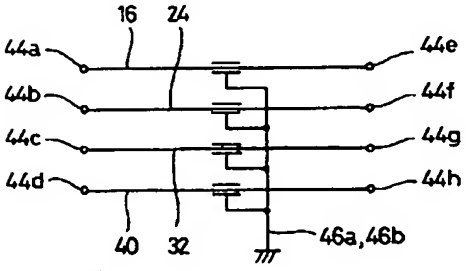
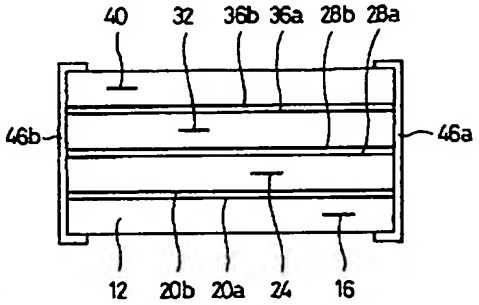
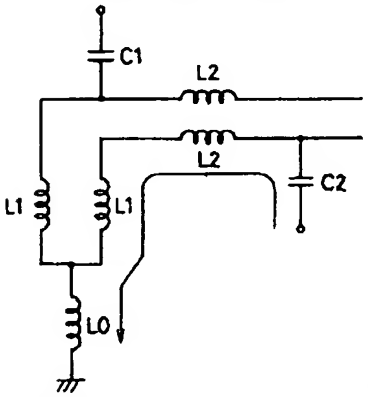
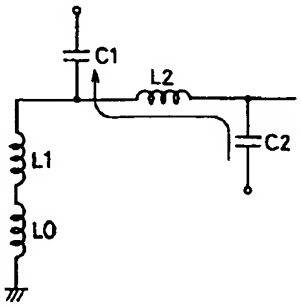


[Drawing 5]



[Drawing 6]





[Drawing 7]

[Drawing 8]

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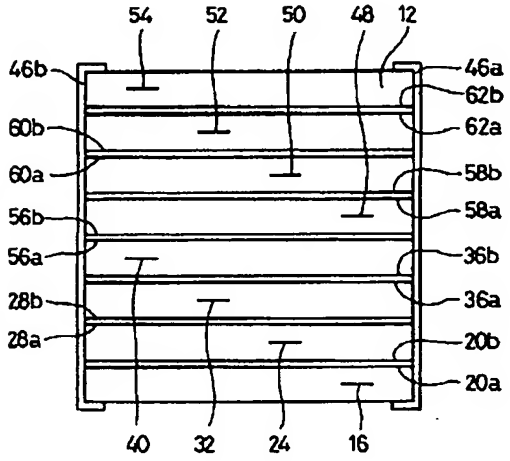
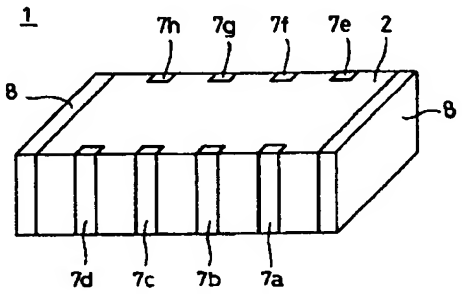
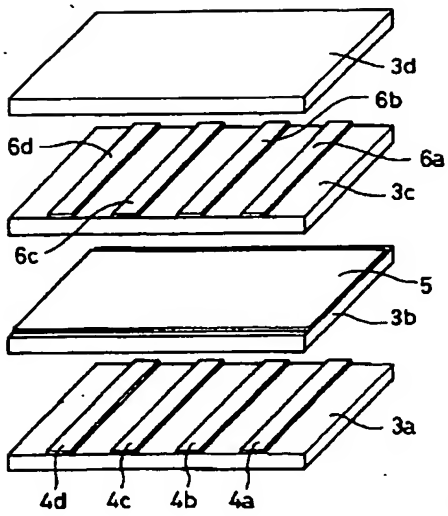


[Drawing 9]



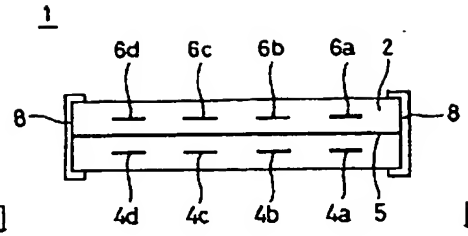
[Drawing 10]

2



[Drawing 11]

1



[Drawing 12]

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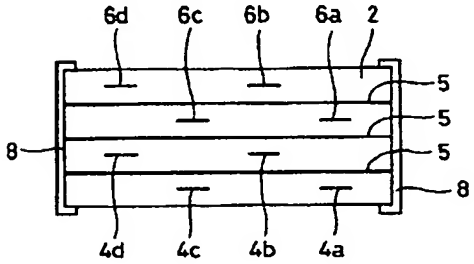

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